MALAVIYA NATIONAL INSTITUTE OF TECHNOLOGY JAIPUR

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Scheme of Master of Technology in VLSI Design

Semester. I

S.No.	Course Code	Course Title	Course Category	Type	Credit	L	T	P
1	ECT601	Digital IC Design	Programme Core	Theory	3	3	0	0
2	ECT621	Advanced Semiconductor Devices	Programme Core	Theory	3	3	0	0
3	ECT633	Analog IC Design	Programme Core	Theory	3	3	0	0
4	ECT912	Reduced order Modeling, Optimization & Machine intelligence	Programme Core	Theory	2	2	0	0
5	ECP611	Semiconductor Devices and IC Simulation Lab	Programme Core	Laboratory	1	0	0	2
6	-	Program Elective (PE-1)	Program Elective	Theory	3	3	0	0
7	-	Program Elective (PE-2)	Program Elective	Theory	3	3	0	0
		Total Credits			18			

Semester. II

S.No.	Course Code	Course Title	Course Category	Type	Credit	L	T	P
1	ECT634	Micro-& Nano- electro-mechanical Systems (MEMS & NEMS)	Programme Core	Theory	3	3	0	0
2	ECP612	System Design Lab	Programme Core	Laboratory	3	0	0	6
3	ECP900	Technical Documentation	Programme Core	Theory	1	0	0	2
4	-	Program Elective (PE-3)	Program Elective	Theory	3	3	0	0
5	-	Program Elective (PE-4)	Program Elective	Theory	3	3	0	0
6	-	Program Elective (PE-5)	Program Elective	Theory	3	3	0	0
7	-	MOOC Course			2/3/4			
		Total Credits			16			

Semester. III

S.No.	Course Code	Course Title	Course Category	Type	Credit	L.	T	P
1	ECD659	Dissertation	Dissertation		6	0	0	12
2	ECD656	Minor Project (Research Project)	Research Project		4	0	0	4
		Total Credits			10			

Semester. IV

S.No.	Course Code	Course Title	Course Category	Type	Credit	L	T	P
1	ECD660	Dissertation	Dissertation		12	0	0	24
		Total Credits			12			

List of Programme Electives

S. No.	Course Code	Course Title	Course Category	Type	Credit	L	T	P
1	ECT614	VLSI Technology	Program Elective	Theory	3	3	0	0
2	ECT616	Computer Arithmetic & Micro-architecture Design	Program Elective	Theory	3	3	0	0
3	ECT618	Graph Algorithms & Combinatorial optimization	Program Elective	Theory	3	3	0	0
4	ECT622	System Level Design & Modeling	Program Elective	Theory	3	3	0	0
5	ECT624	VLSI Testing & Testability	Program Elective	Theory	3	3	0	0
6	ECT626	Formal Verification of Digital Hardware & Embedded Software	Program Elective	Theory	3	3	0	0
7	ECT628	Memory design & testing	Program Elective	Theory	3	3	0	0
8	ECT630	Advanced Computer Architecture	Program Elective	Theory	3	3	0	0
9	ECT631	Digital System Design & FPGA	Program Elective	Theory	3	3	0	0
10	ECT632	Embedded SoC & Cyber Physical Systems	Program Elective	Theory	3	3	0	0
11	ECT638	Design of Asynchronous Sequential Circuits	Program Elective	Theory	3	3	0	0
12	ECT640	Electronic manufacturing Technology	Program Elective	Theory	3	3	0	0

13	ECT642	FPGAs Physical Design	Program Elective	Theory	3	3	0	0
14	ECT644	Mixed Signal IC Design	Program Elective	Theory	3	3	0	0
15	ECT648	Languages for Hardware Description, Scripting and Simulation	Program Elective	Theory	3	3	0	0
16	ECT649	Nanotechnology & Emerging Applications	Program Elective	Theory	3	3	0	0
17	ECT652	RF MEMS	Program Elective	Theory	3	3	0	0
18	ECT654	RF Integrated Circuits	Program Elective	Theory	3	3	0	0
19	ECT656	Adaptive Signal Processing	Program Elective	Theory	3	3	0	0
20	ECT657	VLSI signal processing architectures	Program Elective	Theory	3	3	0	0
21	ECT658	Current-Mode Analog Signal processing	Program Elective	Theory	3	3	0	0
22	ECT703	CAD Algorithms for Synthesis of VLSI Systems	Program Elective	Theory	3	3	0	0
23	ECT736	Medical Engineering & Systems	Program Elective	Theory	3	3	0	0
24	ECT643	Selected Topics in VLSI-1	Program Elective	Theory	1	1	0	0
25	ECT645	Selected Topics in VLSI-2	Program Elective	Theory	1	1	0	0
26	ECT646	Selected Topics in VLSI-3	Program Elective	Theory	1	1	0	0
27	ECT647	Selected Topics in VLSI-4	Program Elective	Theory	1	1	0	0

*MOOC course is over and above the scheme (optional but not mandatory for completion of degree)

Sem I	Taught courses + Lab	17+1=18
Sem II	Taught courses + Lab	16
Sem III	Minor Project (Research Project), Dissertation	4+6=10
Sem IV	Dissertation	12
	Total	56

Programme core	15
Laboratory	4
Programme electives	15
Open elective	00
Minor Project (Research project)	04
Dissertation	18
Total	56

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Program: M. Tech. (VLSI Design)	Department: Electronics & Communication Engineering
Course Code: ECT601	Course Name: Digital IC Design
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Core	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	50%

Syllabus: **Introduction to MOSFETs technology:** Process flow and masking steps for MOS, Electrical behaviour of MOS transistors and CMOS fabrication technologies (well process, SOI and scaling), Latch up in CMOS technology. **[4h].**

CMOS Inverter: Design , analysis of NMOS inverter (resistive, enhancement and depletion load) , CMOS inverters; transfer characteristics, Noise margins, , rationing of transistor size, logic voltage levels, rise and fall of delays, Propagation Delay, Power Consumption. **[6h].**

Combinational Circuits: Design of basic gates in NMOS technology; CMOS logic design styles: static CMOS logic (NAND, NOR gates), complex gates, Pass Transistor logic, Transmission gate, Dynamic MOS design: pseudo NMOS logic, clocked CMOS (C2 MOS) logic, domino logic, NORA, Half and Full adder), Multiplexer, XOR, XNOR **[10h].**

Logical Effort: Logical Effort of Different Digital Circuit Design, Input capacitance, Logical and Electrical effort. parasitic delay, Single stage and Multistage with and without branch network. Design of minimum delay and optimization of best stages.**[5h]**

Layout and stick diagram: Layout Design Rules: Lambda and micron based design rules- stick diagram, Layer properties of various conducting layers in MOS and CMOS technology (diffusion, poly-silicon and metal), Layout design of different CMOS circuit, area estimation.**[5h]**

Sequential MOS Logic and Memory Design: Static latches; Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Memory Design: ROM & RAM cells **[10h].**

Project: Introduction of open source tools: EDA. The class project is to design a reasonably complex CMOS circuit. The project will be performed as a team of two or three students

Text Books:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis and Design, Second Edition, McGraw-Hill, 1999.
2. Rabaey, Chandrakasan and Milokic. Digital system design- A design perspective. Pearson education, India.
3. Neil H.E.Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, A System Perspective, Pearson Education, India. 4. Ken Martin, Digital Integrated Circuits, Oxford Press.
4. CMOS Circuit Design, Layout and simulation: J. Baker, D.E. Boyce., IEEE press.

Course Outcomes: At the end of the course the student will be able to:

CO1- Understand the advancement of CMOS devices and circuits (Cognitive- understanding)

CO2- Design CMOS circuits with specified noise margin and propagation delay. (Skills- Evaluate)

CO3- Implement efficient techniques at circuit level for improving power and speed of combinational and sequential circuits. (Skills- Analyze)

CO4- Design and optimization of layout for Digital ICs. (Skills-Creating)

Program: M. Tech. (VLSI Design)	Department: Electronics & Communication Engineering
Course Code: ECT621	Course Name: Advanced Semiconductor Devices
Credit: 3	L-T-P: 3-0-0

Pre-requisite Course: None

Course Type: Core

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment) 20%
(ii) Mid-term examinations 30%
(iii) End Semester Examination 50%

Syllabus:

Basic Semiconductor Physics : Crystal lattice, energy band model, density of states, distribution statics – Maxwell-Boltzmann and Fermi-Dirac, doping, carrier transport mechanisms, drift, diffusion, thermionic emission, and tunneling: excess carriers, carrier lifetime, recombination mechanisms – SHR, Auger. **[6h]**

P-N Junction and Metal-Semiconductor Junction: p-n junctions- fabrication, basic operation – forward and reverse bias, DC model, charge control model, I-V characteristics, steady-state and transient conditions, capacitance model, reverse-bias breakdown, SPICE model; metal-semiconductor junctions –fabrication, Schottky barriers, rectifying and ohmic contacts, I-V characteristics. **[6h]**

MOS Capacitors and MOSFETs: The MOS capacitor – fabrication, surface charge, accumulation, depletion, inversion, threshold voltage, C-V characteristics – low and high frequency; MOSFET – fabrication, operation, gradual channel approximation, simple charge control model (SCCM), Pao-Sah and Schichman – Hodges models, I-V characteristics, second-order effects – Velocity saturation, short-channel effects, charge sharing model, hot-carrier effects, gate tunneling: subthreshold operation – drain induced barrier lowering (DIBL) effect, unified charge control model(UCCM), SPICE level 1, 2, and 3, and Berkeley short-channel model (BSIM). **[8h]**

MESFET and HEMTs: fabrication, basic operation, Shockley and velocity saturation models, I-V characteristics, high-frequency response, backgating effect, SPICE model; HEMTs – fabrication, modulation (delta) doping, analysis of III-V heterojunctions, charge control, I-V characteristics, SPICE model. **[8h]**

Advanced MOSFET technology: Partially and fully depleted SOI MOSFETs, high-k MOS devices, strained technology, metal gate electrode, FinFETs and Multi gate MOSFETs, enhanced quasi ballistic transport, Si Nanowire MOSFETs. **[10h]**

Text Books:

1. Physics of Semiconductor Devices: *S. M. Sze, Wiley Eastern, (1981).*
2. Semiconductor physics and Devices, Donald Neamen, McGraw-Hill, 3rd edition.
3. Solid State Electronic Devices ,B.G.Streetman and S.Banerjee ,Prentice Hall India.
4. CMOS Circuit Design, Layout and simulation: *J. Baker, D.E. Boyce., IEEE press.*

Course Outcomes:

At the end of the course the student will be able to:

CO1- Understand the physical behavior of semiconductor devices. (Cognitive-Understanding)
CO2- Identify challenges of scaling in semiconductor devices. (Cognitive- Applying)
CO3- Compare performance metrics of semiconductor devices at different technology nodes. (Skills- Evaluate)
CO4- Design and Optimization of devices for low power and high performance circuits. (Affective- Create)

Program: M. Tech. (VLSI Design)	Department: Electronics & Communication Engineering
Course Code: ECT633	Course Name: Analog IC Design
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Core	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	50%

Syllabus:

Introduction to analog VLSI and analog design issues in CMOS technologies[1h]

Basic MOS Device Physics: Structure of MOSFET, Operation of MOSFET, MOS Device Models, **Active** resistors, current, voltage sources and sinks, Bandgap Text Books.[3h]

Amplifiers: Common Source, Source follower, Common Gate and Cascode amplifiers, Biasing Techniques[10h]

Differential Amplifier-Basic differential Pair, common mode response, CMRR, Differential Pair with MOS load, Gilbert Cell [5h]

Current Mirror- Basic Current Mirrors, Cascode Current mirror, Active Current mirror[4h]

Frequency Response of Amplifiers: Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers, Cascode stage, Differential pair[6h]

Noise: Types of Noise, Noise in Single stage amplifiers, Current Mirrors, Differential pair[4]

OPAMP Design: Single stage and Two Stage OPAMP, Stability and Frequency compensation [4-6h]

Text Books:

1. Design of Analog CMOS Integrated Circuits: Behzad Razavi,McGraw Hill Education(India) Edition 2018
2. CMOS Circuit Design, Layout and simulation: J. Baker, D.E. Boyce., IEEE press (2010).
3. VLSI Design techniques for Analog and digital Circuits: R.L. Geiger, P.E. Allen, D. R. Holberg, OUP, (2/E) McGraw Hill (2002)
4. VLSI Design techniques for Analog and digital Circuits: Randel Geiger, P Allen, N Strader, Tata Mcgraw, Hill, (2/E) (2010)
5. Analysis And Design Of Analog ICs : Paul R. Gray, Paul J. Hurst Stephen H. Lewis, Robert G. Meyer, J, Willy and Sons. (4/E) (2001)

Course Outcomes:

At the end of the course the student will be able to:

CO1: Analyze and design amplifiers, current mirrors and differential amplifiers. (Skills- Analyze)

CO2: Understand the significance of different biasing techniques and apply them aptly to different circuits. (Cognitive- Understanding)

CO3: Comparatively evaluate the frequency response of single stage amplifiers, cascode amplifiers and differential amplifier circuits (Cognitive- Analyze)

CO4: Analyze and design two stage operational amplifier circuits (Skills- Create)

CO5: Understand basics of noise in different amplifier circuits (Cognitive- understand)

CO6: Analyze & design the compensation method of operational amplifiers for stability. (Skills- Evaluate)

Program: M. Tech. (VLSI Design)	Department: Electronics & Communication Engineering
Course Code: ECT 912	Course Name: Reduced order Modeling, Optimization & Machine intelligence
Credit: 2	L-T-P: 2-0-0

Pre-requisite Course: None

Course Type: Core

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components,

    (i) Weekly Submissions (Internal assessment)   20%

    (ii) Mid-term examinations   30%

    (iii) End Semester Examination   50%

Syllabus:

A. **Reduced order modelling & large Eigen value methods-**

(i) (a) Large Matrix analysis and large Eigen value problem– Groups, fields and rings; vector spaces; basis & dimensions; canonical forms; inner product spaces- orthogonalization, Gram-Schmidt orthogonalization, unitary operators, change of orthonormal basis, diagonalization; (b) Eigenvalues & eigen vectors- Gerschghorin theorem, iterative method, Sturm sequence, QR method, introduction to large eigen value problems.   06 Hrs.

(ii) Reduced order modelling of systems- Taylor's polynomial, least square approximation, Chebyshev series/polynomial, curve fitting & splines, Pade& rational approximation   04 Hrs.

B. **Discrete Structures, algorithms & Combinatorial optimization-** counting methods, algorithm analysis, graph algorithms, dynamic algorithms, randomized algorithms, probabilistic algorithms, combinatorial optimization   10 Hrs.

C. **Digital arithmetic & machine intelligence-**

(i) Number theory & computer arithmetic- unconventional number systems, residue number system, logarithmic number system, Chinese remainder theorem; fast evaluation of elementary & transcendental arithmetic functions.   06 Hrs.

(ii) Preface to AI- first order logic & inferencing, uncertainty, probabilistic reasoning systems, making decisions under uncertainty.   04 Hrs.

Suggested Text Books (not limited to)-

1. Schaum's outline on Linear Algebra, McGraw Hill
2. Topics in Algebra, I. N. Herstein, Wiley.
3. Advanced Model Order Reduction Techniques in VLSI Design, Sheldon Tan, Lei He, Cambridge Univ. Press, 2007.
4. Model Order Reduction: Theory, Research Aspects and Applications edited by W. H. A. Schilders, Henk A. Van Der Vorst, Joost Rommes, Springer.
5. Gerald, C F; Wheatley P O; Applied Numerical Analysis, Pearson, 2017
6. Theory and Applications of Numerical Analysis, G. M. Phillips, Peter J. Taylor, Academic press
7. Discrete Structures, Schaum outline
8. Cormen, Rivest, Leiserson, Introduction to Algorithms, PHI
9. Combinatorial optimization, Papadimitriou and Steiglitz, PHI (I)
10. Israel Koren, Computer Arithmetic- Academic Press
11. Russel and Norvig- Artificial Intelligence: A Modern Approach, Pearson, 3rd Ed. 2017

Further Text Books

1. Luigi FORTUNA, Guiseppe NUNNARI, Antonio GALLO, MODEL ORDER REDUCTION TECHNIQUES WITH APPLICATIONS IN ELECTRICAL ENGINEERING, Springer, 1992.
2. Y. Saad, Numerical methods for large Eigenvalue problems, www.umn.edu
3. Matrix Analysis & linear algebra, Meyer, SIAM
4. H. A. van der Vorst, Iterative methods for large linear systems, citeseerx.ist.psu.edu

5. Cheng et al. Symbolic analysis and reductions of VLSI circuits, Springer, 2005

Course outcomes

CO1. Is able to grasp core concepts, basic tenets of linear algebraic structures- groups, fields and rings;vector spaces (knowledge)

CO2. Is able to grasp features, properties and operations on vector spaces- orthogonalization, change of basis, diagonalization (knowledge)

CO3. Is able to learn & apply problem solving for computing eigen values and eigen vectors etc. (Thinking, skills)

CO4. Is able to demonstrate application of algorithms (Gerschgorin, Sturm sequence method, QR method) for eigen value computation/estimation and MATLAB/SCILAB validation(skills)

CO5. Is able to describe algorithms for function approximation, fitting (rational, Chebychev, Pade etc.) using MATLAB (skills)

CO6. Develops appreciation for combinatorial optimization algorithms. AI probabilistic approaches & implements through MATLAB/C++/SCILAB (skills)

Program: M. Tech.	Department: Electronics & Communication Engineering
Program: M. Tech. (VLSI Design)	Department: Electronics & Communication Engineering
Course Code: ECP611	Course Name: Semiconductor Devices and IC Simulation Lab
Credit: 1	L-T-P: 0-0-2
Pre-requisite Course: None	
Course Type: Core	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components:

(i) Weekly Submissions (Internal assessment)	50%
(ii) Mid-term examinations	00%
(iii) End Semester Examination	50%

Syllabus:

(a) VLSI TCAD Experiments

1. Design and Simulation of 2D/3D NMOS Channel Length 20nm or higher.

2. Design and Simulation of 2D/3D PMOS Channel Length 20nm or higher

3. Implementation of SOI/Bulk 2D/3D Nanowire FET & Tunnel FET using TCAD.

4. Implementation of SOI/Bulk Dual Gate FET & Dual Gate Junctionless FET.

5. Design and Implementation of SOI/Bulk FINFET device upto 5nm technology using GDS2MESH and GENIUS.

(b) Digital and Analog ICs Experiments

1. I-V characterization of N-MOSFET and P-MOSFET for long and short channel models.
2. VTC and Transient Analysis of CMOS Inverter for different W/L Ratio of NMOS and PMOS.
3. Simulation and Analysis of NMOS based Inverter circuits such as Diode Connected Load, Depletion Load and PMOS Load.
4. Connect a 2 I/P NAND Gate to an identical NAND Gate such that fan out is 1,2,5,10,50,100. Plot the propagation Delay.
5. Connect a set of 5 inverters in a closed loop in the form of a clock. Estimate the clock frequency.
6. To design layout of CMOS inverter and followed by simulation.
7. To design layout of 2 input NAND/NOR and followed by simulation.
8. To find 3 dB frequency & gain for different values of load & W/L ratio for common source stage with resistive load using P-MOSFET.
9. Simulation & analysis of diode-connected load common source amplifier. Find edge of triode region & gm1, gm2, gain & 3 dB frequencies.
10. DC analysis of source follower using resistive & current source load.
11. AC analysis of common gate amplifiers and calculates input and output impedance.
12. AC analysis differential amplifier & calculate CMRR.
13. Design 2 stage OPAMP for the given specification.
14. Simulation of basic current mirrors using resistive load and cascode current mirror.

Course Code: ECT634	Course Name: Micro& Nano Electro Mechanical System (MEMS & NEMS)
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Core	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%	
(ii) Mid-term examinations	30%	
(iii) End Semester Examination	50%	

Syllabus:

Introduction to MEMS: Introduction: micro- and nano-scale size domains; scaling of physical laws; MEMS materials and processes; Miniaturization Issues. MEMS devices and applications, MEMS Market **[4h]**.

MEMS Fabrication Technology: Introduction to Submicron Technology: semiconductor materials; photolithography; doping; thin film growth and deposition; CVD, lithography and Ion Implantation, metallization; wet and dry etching; silicon micromachining; Bulk micromachining; Surface micromachining and LIGA **[4h]**.

MEMS Sensors and Actuators (Electrostatic, Thermal, piezoresistive): mechanics including elasticity, beam bending theory, membranes/plates; microactuators based on various principles, electrostatic, thermal, piezoresistive and applications e.g. acceleration, strain, tactile, temperature, IR detector flow; inkjet **[10h]**.

MEMS Sensors and Actuators (RF and Bio): MEMS Sensors and Actuators: mechanics including piezoelectric, magnetic, optical and its application. e.g. Microphone, micro speaker, nanogenerator, micro-motor, RF resonator, SAW filter. Materials and processes for BioMEMS, Applications **[10h]**.

MEMS Devices Packaging and Calibration: MEMS device Calibration and packaging techniques, Reliability. MEMS software training: COMSOL &Intellisuite **[12h]**.

Project

The class project is to design reasonably complex MEMS devices. The project will be performed as a team of two or three students

Text Books:

1. Course notes – will be posted weekly on the course website
2. Foundations of MEMS, Chang Liu. Prentice Hall (2006)
3. Fundamentals of Micro fabrication, Marc Madou, CRC (2002)
4. Introduction to BioMEMS – Albert Folch, CRC (2012)

Course Outcomes:

At the end of the course the student will be able to:

CO1- Gain a knowledge of basic approaches for various MEMS sensors and actuators design. (Cognitive-understaning)

CO2-Capability to critically analyze microsystems technology for technical feasibility as well as practicality. (Affective- Evaluate)

CO3 -Develop efficient design for improving device performance in terms of speed, sensitivity Selectivity and accuracy. (Skills- Create)

CO4- Design and optimization of RF MEMS sensors and actuators (Skills- Create)

CO5- Design and analysis of efficient MEMS presser sensor. (Skills- Analyze)

Program: M. Tech. (VLSI Design)	Department: Electronics & Communication Engineering
Course Code: ECP612	Course Name: System Design Lab
Credit: 3	L-T-P: 0-0-6
Pre-requisite Course:	
Course Type: Core	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	50%
(ii) Mid-term examinations	00%
(iii) End Semester Examination	50%

Syllabus:

Course Content:
1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. Encoder/ Priority Encoder
4. Code Converter
5. Flip-flop
6. Shift Register/ Universal Shift Register
7. Comparator
8. Upcounter/ Downcounter
9. Memory – ROM, RAM
10. Array Multiplier/ Array Multiplier With Pipelining
11. FIR Filter

Python Programming, HDL Programming, Experiments on CPLD, FPGA, Layout Design

Course Outcomes:

CO1: Simulate adders, multiplexers, code converters for the given specifications.
CO2: Evaluate the performance for the design parameters.
CO3: Design and test memory elements.
CO4: Use pipelining for efficient multiplier designs.
CO5 Apply pipelining for efficient FIR filter designs.

Program: M. Tech. (VLSI Design)	Department: Electronics & Communication Engineering
Course Code: ECP 900	Course Name: Technical Documentation
Credit: 2	L-T-P: 0-0-2
Pre-requisite Course: None	
Course Type: Core	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	50%

Syllabus:

Introduction: Literature survey – Understanding journal metrics (impact factor, number of citations, h-index, i10 index), Identifying high impact articles, Problem identification, Ethics of publishing.

(2 hours)

Document Formatting: Advantages of LaTeX, Installation, Package manager, Editors, Typesetting, Classes – Book, Thesis, Article, Slide, Poster, Parts of a document - Chapters, Sections, Items, Fonts, Acronyms, Author kits, Debugging.

(8 hours)

Figures, Tables, and Equations: Figures, Subfigures, Tables, Types of tables, Spacing in tables, Captions, Equations, Equation arrays, Equation numbering, Labels.

(8 hours)

Referring articles: Using labels, Citing articles, Bibliography, Bibtex, Styles, Mendeley, JabRef.

(4 hours)

Artwork: Drawing with LaTeX, Flowcharts in LaTeX, Creating plots with Gnuplot/ Octave/ Matlab, Creating scalable vector graphics with Inkscape, Tikz.

(4 hours)

Reformatting documents, Responding to reviewer comments, Reviewing technical documents. (2 hours)

References:

1. World wide web

Similar courses at:

https://www.anadolu.edu.tr/en/academics/faculties/course/99276/documentation-with-latex/content (3 credit) Anadolu University, Turkey

https://www.training.cam.ac.uk/course/ucs-latex (2 half days) Cambridge, UK

http://uva-fnwi.github.io/LaTeX/ (4 weeks) University of Amsterdam, Netherlands

https://www.bath.ac.uk/guides/getting-started-with-latex-an-introductory-course-for-doctoral-students/ (6 Hours) University of Bath, UK

Outcomes – The students will be able to

1. Identify high impact literature, understand the importance of ethical publishing
2. Use LaTeX to compile technical documents containing quality figures, tables, and equations.
3. Use bibtex for automatic referencing.
4. Create quality graphics.
5. Understand the process of responding to reviewer comments, and reviewing technical documents.

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT614	Course Name: VLSI Technology
Credit: 3	L-T-P: 3-0-0

Pre-requisite Course: None

Course Type: Elective

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	50%

Syllabus:

Crystal growth & wafer preparation: Processing considerations: Chemical cleaning, getting the thermal Stress factors etc.

Epitaxy: Vapors phase Epitaxy Basic Transport processes & reaction kinetics, doping & auto doping, equipments, & safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.**[10h]**

Oxidation

Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates thin oxides, Oxides, Oxidation technique & systems dry & wet oxidation. Masking properties of SiO_2.**[56h]**

Diffusion

Diffusion –kinetics, Fick's law, sheet resistivity, methods of diffusion. Diffusion from a chemical source in vapor form at high temperature, diffusion from doped oxide source, diffusion from an ion implanted layer.**[6h]**

Lithography

Optical Lithography: optical resists, contact & proximity printing, projection printing, electron lithography: resists, mask generation. Electron optics: roster scans & vector scans, variable beam shape. X-Ray, e-beam lithography. **[6h]**

Etching

Reactive plasma etching. AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide. Trench etching,**[6h]**

Thin Film Materials & their Deposition: Interlayer dielectrics in microelectronic devices, interconnections within and between different electronic devices. **Packaging of Microelectronic Devices**: Packaging materials, different types of packaging, Microelectronic devices reliability. [6h]

Text Books:

5. S. M. Sze, "VLSI Technology", McGraw Hill.
6. May, Sze, "Fundamentals of Semiconductor Fabrication", Wiley
7. Stephen A. Campbell, "The Science and Engineering of Microelectronic Fabrication", Oxford University Press, 1996.
8. Hong Xiao, "Introduction to Semiconductor Manufacturing", Prentice Hall, 2001.
9. SK Gandhi, "VLSI Fabrication Principles", John Wiley 1983.
10. AB Glaser, GE Subak-Sharpe, "Integrated Circuit Engineering", Reading MA, Addison Wesley 1977.
11. D. Nagchoudhuri, "Principles of Microelectronic Technology", Wheeler Publishing, 1998.

12. Plummer, Deal , Griffin, 'Silicon VLSI Technology: Fundamentals, Practice and Modeling' , Pearson
13. Research papers published in Applied Physics Letters and IEEE journals.

Course Outcomes:

CO1   An understanding of silicon and GaAs electronic device fabrication processes

CO2   Learn different types of operations involved in converting silicon wafer into a complex integrated circuit. Learn in detail basics of all operations used to manufacture a silicon-based monolithic integrate circuit.

CO3   Gain experience in the modelling and simulation of semiconductor manufacturing processes.

CO4   Develop an understanding of the working principle and operational details of semiconductor measurement device.

CO5   Develop an understanding of industrially relevant and research intensive methods of electronic device fabrications. Students should develop understanding of silicon growth methods, thin film growth technologies, lithography and etching processes.

CO6   Become proficient in the measurements of key electrical parameters and characteristics of integrated circuits

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT616	Course Name: Computer Arithmetic & Micro-architecture Design
Credit: 3	L-T-P: 3-0-0

Pre-requisite Course: None

Course Type: Elective

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

    (i) Weekly Submissions (Internal assessment)   20%

    (ii) Mid-term examinations   30%

    (iii) End Semester Examination   50%

Syllabus:

1. Computer arithmetic- conventional & higher radix number systems, residue & logarithmic number systems; sequential & parallel (and high speed) algorithms for addition, multiplication, division; evaluation of elementary functions- sin, cos, sin-1, cos-1, sinhetc; CORDIC method for trigonometric functions. **[12 hrs]**
2. languages for design description (HDLs) like VHDL or Verilog; Modeling and simulation of circuits at various levels; **[10 hrs]**
3. Data path design for high performance- pipelining & systolic arrays; Control design- sequential, hardwired & micro-programmed control. **[10 hrs]**
4. Topics in design-yield and redundancy, Low power design techniques. **[6 hrs]**

Text Books:

For Review

    1. Kohavi, Switching & finite automata theory, Mc Graw Hill

Computer arithmetic

    2. Ercegovac, Digital Systems, Wiely, 2004

    3. Parhami, Computer Arithmetic- Algorithms & Hardware Design, Oxford Univ. Press

    4. Koren, Computer Arithmetic Algebra, Prentice Hall Inc.

For Data-path/Control Design

    5. Hayes, J P, Computer Architecture & organization, Mc Graw Hill, 2003

For HDLs

    6. Navabi. Introduction to VHDL. Mc Graw Hill, 2000

    7. Bhaskar. VHDL Primer. Prentice Hall India, 2001

    8. Navabi. Verilog digital systems. Mc Graw Hill, 2000

    9. Palnitkar, Verilog.... .. Pearson India/Prentice-Hall India

Low power design

    10. Chandrakasan, A. P. Low-power design methodologies. IEEE Press, 1998.

    11. Mead & Conway, VLSI circuit design

    12. Raguram, R. Modeling and Simulation of Electronic circuits. PHIndia, 1996.

    13. Weste and Eshraghian. Principles of CMOS VLSI design. Addison Wesley, 1998.

    14. K. Roy and et al, Low power design, Wiley

Course Outcomes:

CO1: To understand the radix number system (Cognitive - understanding)

CO2: To learn the sequential & parallel algorithm for computer arithmetic (Cognitive - understanding)

CO3: To understand the CORDIC method for evaluation of elementary functions (Skills- Analyze)

CO4: To learn basic concepts in HDLs (Skills- Design)

CO5: To understand basics of data path and control path design methods (Skills- design)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT618	Course Name: Graph Theory and Combinatorial Optimization
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components:

    (i) Weekly Submissions (Internal assessment)   20%

    (ii) Mid-term examinations   30%

    (iii) End Semester Examination   50%

Syllabus:

Graph Theory- basics, Planarization, triangulation, graph algorithms for shortest/longest paths, spanning tree, search etc. [8 hrs]

Optimization problem- Convex sets and functions. The SIMPLEX algorithm- forms of linear programming problem, geometry of LP, organization of Tableau. Computational considerationsfor simplex algorithm [10 hrs]

Duality- dual of LP, dual simplex problem. Primal-dual algorithm. [8 hrs]

Algorithms & complexity- shortest path, max-flow, Dijkshtra's algorithm, min-cost flow, algorithm for graph search and matching; spanning trees and matroids; Integer Linear programming, Greedy algorithm, approximation algorithms; branch-and-bound; dynamic programming. [10 hrs]

Text Books:

1. Narsingh Deo, Graph theory, Prentice Hall India, 2008.
2. T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms." McGraw-Hill, 2007
3. S. Baase, Computer algorithms, Pearson India 2008.
4. Papadimitriou and Steiglitz, Combinatorial optimization, PH India, 2001.
5. Nemhauser and Wolsey, Integer and Combinatorial optimization, Wiley Inter-science 1999.

Course Outcomes:

CO1. Is able to grasp and analyze features, properties of graph entities e.g.cutset, tree, chord-set, cycles etc (Cognitive-Analyze)

CO2. Is able to learn & apply graph algorithms and its applications into Circuits, computer problem solving etc. (Skills- Analyze)

CO3. Is able in long perspective, to appreciate the significance of GRAPH as a versatile modeling entitiy; and the significance that it can be used for analysis, problem solving as well as synthesis- especially for chip design, wireless communication protocols & system design, computer problem solving, data structures etc. (Affective/Skills- Evaluate)

CO4. Is able to write small C/C++ programmes related to implementation of graph algorithms (Skills- Apply)

CO5. Is able to write efficient algorithms for graph-search, and other approximation algorithms (Skills, Evaluate)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT622	Course Name: System Level Design & Modeling
Credit: 3	L-T-P: 3-0-0

Pre-requisite Course: None

Course Type: Elective

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	50%

Syllabus:

UNIT 1. Introduction: Embedded systems, electronic system-level (ESL) design, Models of Computation (MoCs): finite state machines (FSMs), dataflow, process networks, discrete event [6 hrs]

UNIT 2. System-level design languages (SLDLs): SpecC, SystemC. System specification, profiling, analysis and estimation. System-level design: partitioning, scheduling, communication synthesis [10 hrs]

UNIT 3. System-level modeling: processor and RTOS modeling, transaction-level modeling (TLM) for communication. System-level synthesis: design space exploration (DSE) [8 hrs]

UNIT 4. Embedded hardware and software implementation: synthesis and co-simulation, case study. Application specific processors, Retargetable compilers, instruction set-simulation and co-simulation. [8 hrs]

UNIT 5. System design examples and case studies. . Recent trends in system level design and modeling [6 hrs]

Text Books:

5. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Embedded System Design: Modeling. Synthesis, Verification,
6. Springer, September 2009. ISBN 978-1-4419-0503-1, ("Orange book", authors' site).
7. Gerstlauer, R. Doemer, J. Peng, D. Gajski, "System Design: A Practical Guide with SpecC",
8. Kluwer Academic Publishers, Boston, June 2001. ISBN 0-7923-7387-1 ("Yellow book")
9. T. Groetker, S. Liao, G. Martin, S. Swan, "System Design with SystemC", Kluwer Academic Publishers. Boston, May 2002. ISBN 1-4020-7072-1 ("Black book")
10. F. Vahid, T. Givargis, "Embedded System Design: A Unified Hardware/Software Introduction" (authors' site).
11. John Wiley & Sons, 2001. ISBN 978-0-471-38678-0

Course Outcomes:

At the end of the course the student will be able to:

CO1- To model a problem at system level (Cognitive- Analyze)

CO2- Realize architecture for a design problem (Skills- Create)

CO3 -To model a system in System C language (Cognitive- Analyze)

CO4 -To generate system interface specifications and perform refinement (Skills- Create)

CO5- To appreciate HW-SW Co-design with latest trends (Cognitive- understanding)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT624	Course Name: VLSI Testing & Testability
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components:

(i) Weekly Submissions (Internal assessment)	20%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	50%

Syllabus:

UNIT 1. Introduction to VLSI design flow and need of VLSI testing. Physical Faults and their modeling; Stuck at Faults, Bridging Faults; Fault collapsing; Fault Simulation: Deductive, Parallel, and Concurrent Fault Simulation. Critical Path Tracing [10 hrs]

UNIT 2. ATPG for Combinational Circuits: D-Algorithm, Boolean Differences, PODEM Random, Deterministic and Weighted Random Test Pattern Generation; Aliasing and its effect on Fault Coverage. [8 hrs]

UNIT 3. PLA Testing, Cross Point Fault Model and Test Generation. Memory Testing- Permanent, Intermittent and Pattern Sensitive Faults, Marching Tests; Delay Faults. [6 hrs]

UNIT 4. ATPG for Sequential Circuits: Time Frame Expansion ; Controllability and Observability Scan Design, BILBO , Boundary Scan for Board Level Testing ; BIST and Totally self checking circuits. [8 hrs]

UNIT 5. System Level Diagnosis & repair- Introduction; Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes. Latest trends in VLSI Testing and Testability [6 hrs]

UNIT 6. Advance topics on VLSI Testing and Verification

.Text Books:

6. Abramovici, M., Breuer, M. A. and Friedman, A. D. Digital systems testing and testable design. IEEE press (Indian edition available through Jayco Publishing house), 2001.
7. Bushnell and Agarwal, V. D. VLSI Testing. Kluwer.
8. Agarwal, V. D. and Seth. S. C. Test generation for VLSI chips. IEEE computer society press.
9. Hurst, S. L. VLSI testing: Digital and mixed analog/digital techniques. INSPEC/IEE, 1999.

Course Outcomes:

At the end of the course the student will be able to:

CO1: To able to grasp core concepts of digital system testing and testability. (Cognitive- Understanding)

CO2: To understand how a faulty circuit may cause disasters and affect the nature as well as society. (Affective- Analyze Attitude & Value)

CO3: To understand fault detection using different fault simulation techniques. (Skills- Evaluate)

CO4: To develop ability to design algorithms for automatic test generation for combinational circuits, sequential circuits, PLAs and memory. (Skills/Affective- Create)

CO5: To apply probabilistic approaches for random test generation. (Skills- Apply)

CO6: To apply different redundancy based fault tolerance techniques to increase circuit reliability. (Skill/Affective- Analyze)

CO7: To design BIST for a CUT in Verilog/HDL and implement ATPG algorithms in C/C++/MATLAB. (Skills- Create)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT626	Course Name: Formal Verification of Digital Hardware & Embedded Software
Credit: 3	L-T-P: 2-1-0
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components:

(i) Weekly Submissions (Internal assessment)	20%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	50%

Syllabus:

UNIT 1. Introduction to Design Verification, OVM and UVM methodology. case studies using Verilog and SystemVerilog [12 hrs]

UNIT 2. Static verification, Formal Verification of digital hardware systems- BDD based approaches. functional equivalence, finite state automata, FSM verification, Model checking [8 hrs]

UNIT 3. Various industry & academia CAD tools for formal verification. [8 hrs]

UNIT 4. Verification, validation & testing - Debugging techniques for embedded software, instruction set simulators, clear box technique, black box testing, evaluating function test [8 hrs]

UNIT 5. Recent trends in Design verification, case study. [6 hrs]

Text Books:

1. Embedded systems Design- Artist Roadmap for Research & Development, LNCS-3436, Springer.
2. J. W. Valvano, Eembedded microcomputer systems- Real Time Interfacing, , Thomson press (Cengage India)
3. Computers as components- Principles of embedded computing system design. Wolf, W., Academic Press (Indian edition available from Harcourt India Pvt. Ltd., 27M Block market. Greater Kailash II, New Delhi-110 048.)
4. Verification, validation & testing in software engineering. A. Dasso and A. Funes, Idea Group Inc.
5. Advanced Formal Verification, R. Drechsler, Kluwer.
6. Hardware-Software codesign for data flow dominated embedded systems, R. Niemann, Springer.
7. Readings in Hardware/Software codesign, Micheli, Ernst, Wolf, Morgan Kaufmann.

Course Outcomes:

At the end of the course the student will be able to:

CO1: To understand features of System Verilog (Cognitive- Understanding)

CO2: To study Assertion Based Verification and also be aware of functional coverage. (Cognitive-Analyze/Evaluate)

CO3: To apply language constructs of Bluespec for high level design/synthesis. (Skills- Apply)

CO4: To understand the necessity of the verification methodology. (Affective- understanding)

CO5: Ability to develop the test bench for DUT with verification methodology for scheduling. resource sharing and binding.(Skills- Creativity)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT628	Course Name: Memory Design & Testing
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

    (i) Weekly Submissions (Internal assessment)   20%
    (ii) Mid-term examinations   30%
    (iii) End Semester Examination   50%

Syllabus:

Processing technology for Memories: Multiply Floating Gate and Control Gate, Trench Capac itors and thin Oxide. Memory Modeling and testing faults in SRAMs, Marching Tests; Delay Faults. [6 hrs]

Semiconductor memory architecture, Space of memory faults- fault primitives. [6 hrs]

Preparation of Circuit Simulation: Definition & location of open, short, and bridge fault, Simulation methodology. Test for single cell and two port SRAMs, Functional fault modeling and testing of RAMS, [8 hrs]

Fault Diagnosis & Repair Algorithms. [4 hrs]

Built –in self Test and design for testability of RAMs. Built in self repair architecture. [6 hrs]

Trend in Embedded Memory testing. [4 hrs]

Text Books:

1. Pinaki Mazumder, Kanad Chakraborty, Testing and Testable Design of High-Density Random-Access Memories (Frontiers in Electronic Testing), Kluwer academic pub.
2. Said Hamdioui, Testing Static Random Access Memories: Defects, Fault Models and Test Patterns (Frontiers in Electronic Testing), Kluwer academic pub 2004.
3. Pinaki Mazumder and Kanad Chakraborty, Fault –Tolerence and reliability techniques for High –Density Random- Acess Memories, Pearson India, 2002..

Course Outcomes:

CO1: To know the basics of evaluation of elementary functions (Cognitive- Understand)

CO2: to understand fundamentals of Memory Modeling and testing faults (Cognitive- Understand)

CO3: To learn the techniques and algorithm for testing and fault diagnosis (Skills- Evaluate)

CO4: To understand basics of built-in self test and related issues (Skills- Design)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT630	Course Name: Advanced Computer Architecture
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	50%

Syllabus:

- Advance micro-architecture & Instruction level parallelism- pipelining & superscalar techniques; Instruction formats, instruction sets and their design, Pipelining; dynamic scheduling, VLIW, EPIC; [8 hrs]

- Memory hierarchy; Bus cache & shared memory; multilevel cache design & performance; memory systems and error detection and error correction coding; [8 hrs]

- Data level parallelism- parallel and superscalar architectures- multivector, SIMD, GPU, CUDA/OpenCL programming etc.; heterogeneous SoC processors: [8 hrs]

- Thread level parallelism- scalable multithreaded architectures, Simultaneous multithreaded architectures (SMT); multicore; hyper threading; dataflow, cluster architectures. VLIW, RISC, [8 hrs]

- parallel program development and environments; [4 hrs]

Text Books:

1. D. Patterson and J. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufmann Publishers, Inc.. Second edition, 1998.
2. Computer Architecture: A Quantitative Approach, John L. Hennessy & David A Patterson, Morgan Kaufmann, 1996.
3. Structure Computer Organization, 4th Edition, Andrew S. Tanenbaum, Prentice Hall, 1999.
4. Computer Architecture and Organization, J. Hayes, McGraw Hill, 1988.
5. Computer Organization and Architecture. 5th Edition, William Stallings, Prentice Hall, 1996.

Course Outcomes:

A student who has successfully completed this course should be able to:

CO1: Analyze various performance characteristics of a computer system & trade-offs involved (cognitive- Analyze)

CO2: Apply digital design techniques to the microarchitecture construction of a processor (Skills- Apply)

CO3: understand I/O modules organization and operating system support (Skills- analyze)

CO4: perform the designing of instruction sets architecture (ISA with HW/SW) and evaluate using tools for statistical analysis of instruction set trade-offs (Skills- design)

CO5: Gain the ability to develop parallel GPGPU solutions of CUDA and OpenCL (Skills- analyze)

CO6: Apply knowledge of processor design to improve performance in algorithms and software systems. (Affective- Evaluate)

Program: M. Tech. (VLSI Design)	Department: Electronics & Communication Engineering
Course Code: ECT631	Course Name: Digital System Design & FPGAs
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components:

(i) Weekly Submissions (Internal assessment)   20%
(ii) Mid-term examinations   30%
(iii) End Semester Examination   50%

Syllabus: Sequential Logic Design-Introduction, Basic bistable Memory Devices, additional bistable devices, reduced characteristics and excitation table for bistable devices. [6 h]

Synchronous Sequential Logic Circuit Design- Introduction, Moore, Mealy and Mixed type Synchronous State Machines. Synchronous sequential design of Moore, Melay machines. [9 h]

Asynchronous Sequential Logic Circuit Design- Introduction, analysis and synthesis of asynchronous State Machines. Hazards. [9 h]

Algorithmic State Machine- An Algorithm with inputs, digital solution, Implementation of traffic light controller. ASM charts, Design Procedure for ASMs. [3 h]

Data path and Control design. [3 h]

Introduction to FPGA: Basics of PLD, FPGA Design Tool Flow, Basic blocks of FPGA, State of art architectures of FPGA, Applications of FPGA; FPGA mapping of combinational & sequential designs [6 h]

Text Books:

1. Digital System Design, Ercegovac, Wiley.

2. Richard S. Sandige, *Modern Digital Design*, McGraw-Hill, 1990.

3. ZviKohavi, Switching and Finite Automata Theory, Tata McGraw-Hill.

4. Navabi. Analysis and modeling of digital systems. McGraw Hill, 1998.

5. Perry. Modeling with VHDL. McGraw Hill, 1994.

6. Navabi. Verilog Digital Design. McGraw Hill, 2007.

7. Fundamentals of Digital Logic with Verilog Design, Stephen Brown and ZvonkoVranesic, McGraw Hill, 2002.

Course Outcomes:

CO1: To be able to apply the basic design principles of sequential logic systems. (Cognitive- Applying)

CO2: To understand the design concepts of synchronous and asynchronous state machines in Moore and Mealy architectures. (Cognitive- understanding)

CO3: To analyze & design data path, control path design and various programmable devices (Skills- Create)

CO4: To be able to implement a digital system using HDLs(Skills-Evaluate)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT632	Course Name: Embedded SoC & Cyber Physical Systems
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	50%

Syllabus:

Embedded SoC

Design methodology- high performance embedded computing, and real-time operating system; HW-SW codesign, FPGA for embedded Systems design, programmable SoC (Zynq SoC); Advanced Computing Models & Architectures   [8 hrs]

ARM, interfacing, Microkernels and exokernels, monolithic kernels, Domain specific architectures, Zynq SoC based design methodology- boot image, flash; advanced Cortex™-A9 processor services; DMA controller in the Zynq SoC; Ethernet and USB controllers;   [8 hrs]

(Optional) Software organization, scheduling, and execution; Energy management and low-power design; Safety and reliability in embedded systems; Emerging Memory Technologies; Fault Resilient Chip Design; Energy Efficient ExascaleSystems;   [8 hrs]

Cyber physical Systems

Algorithms, hardware and software components integration with Internet; conceptual understanding of techniques to translate application non-functional requirements to middleware and hardware functionality, as well as practical implementation of these techniques; Interfacing to the external world through sensors and actuators [8 hrs]

(a) Case studies: Low-end systems (medical devices, smart cards, sensors)   [3 hrs]
(b) Case studies: High-end systems (automobiles, home electronics, robotics)   [3 hrs]

Text Books:

1. Jonathan W. Valvano, *Embedded Systems: Real-Time Operating Systems for ARM® Cortex™-M Microcontrollers*, Volume 3, Fourth edition, January 2017, ISBN: 978-1466468863, Outline: http://www.ece.utexas.edu/~valvano/arm/outline3.htm
2. Edward Lee and SanjitSeshia, *Introduction to embedded systems: A cyber-physical systems approach*, MIT Press, 2016. (**Free PDF:** http://leeseshia.org/download.html)
3. Philip Koopman, *Better embedded system software*, Drumnadrochit Education, 2010.
4. *Embedded System Design: A Unified Hardware/Software Introduction*. Frank Vahid and Tony Givargis, John Wiley and Sons, 2001, ISBN No. 04711386782.
5. *High-Performance Embedded Computing: Architectures, Applications, and Methodologies*, Wayne Wolf, Morgan Kaufmann Publishers, 2006, ISBN No. 012369485.
6. J .Fitzgerald, P.G. Larsen, M. Verhoef (Eds.): *Collaborative Design for Embedded Systems: Co-modelling and Co-simulation*. Springer Verlag, 2014. ISBN 978-3-642-54118-6.
7. Suh, S.C., Carbone, J.N., Eroglu, A.E.: *Applied Cyber-Physical Systems*. Springer, 2014.
8. Hennessy and Patterson, Computer Architecture- A Quantitative Approach, 4th or later Edition (ISBN-13: 978-0123704900 ISBN-10: 0123704901 Edition: 4th)

Further reading

1. Edward A. Lee, Cyber-Physical Systems - Are Computing Foundations Adequate?
2. Paulo Tabuada, Cyber-Physical Systems: Position Paper

3. Rajesh Gupta, Programming Models and Methods for Spatio-Temporal Actions and Reasoning in Cyber-Physical Systems
4. E. A. Lee and S. A. Seshia, Introduction to Embedded Systems - A Cyber-Physical Systems Approach, http://LeeSeshia.org, 2011.
5. Altawy R., Youssef A., Security Trade-offs in Cyber Physical Systems: A Case Study Survey on Implantable Medical Devices
6. Ahmad I., Security Aspects of Cyber Physical Systems
7. "US National Science Foundation. Cyber-Physical Systems (CPS)"
8. ^ Jump up to:[a][b] Khaitan et al., "Design Techniques and Applications of Cyber Physical Systems: A Survey", IEEE Systems Journal, 2014.

Course outcomes:

Is able to:

CO1: Understand significance of embedded HW/SW, computing models &architectures (Cognitive- Understand)

CO2: Understanding of CPU operation, I/O devices and their interfacing (Cognitive- Understand)

CO3: Develop C/C++ programs in real-time operating systems for memory management, interrupt handling, thread management, task scheduling and software/hardware interfacing. (Skills- Apply, Create)

CO4: Learn program and system design and analysis methodologies (Skills- analyze and design)

CO5: Relate to the real-world applications of embedded systems and associate it with emerging areas such as Cyber-Physical Systems (CPS), Internet-of-Things (IoT), and robotics.

Laboratory-

Implement an effective Zynq SoC boot design methodology - Create an appropriate FSBL image for flash; Identify advanced Cortex™-A9 processor services for fully utilizing the capabilities of the Zynq SoC; Analyze the operation and capabilities of the DMA controller in the Zynq SoC; Examine the various Standalone library services and performance capabilities of the Ethernet and USB controllers in the Zynq All Programmable SoC; Describe the Standalone library services available for low-speed peripherals that are contained in the Zynq PS.

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT638	Course Name: Design of Asynchronous Sequential Circuits
Credit: 3	L-T-P: 3-0-0
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations	

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%	
(ii) Mid-term examinations	30%	
(iii) End Semester Examination	50%	

Syllabus:

Introduction: Summary of synchronous techniques - disadvantages in today's technology. Advantages of asynchrononous techniques - low power, performance, modularity. Historic difficulties with asynchronous design. Flow Table Reduction, The state-assignment Problem, Delays, Hazards, and Analysis, Feedback, other Modes of operation, Counters. [10 hrs]

Circuit Classification: Bounded Delay, speed independent, and delay independent. Data models (single-rail, dual-rail). Handshaking protocols (2 phase, 4 pase)nd without data processing elements. The design of the Amulet processors. [8 hrs]

NCL Logic: The NULL convention logic approach. Preserving delay insensitivity, threshold gates with hysteresis. [6 hrs]

Formal Aspects of Asynchronous: The Rainbow appr [6 hrs]

MicropipelineCircuits: Basic building blocks. Pipelines, with aoach. Green descriptions of micro-pipelines. Overview of formal basis to asynchronous descriptions [6 hrs]

Text Books:

1. Asynchronous sequential circuits by Stephen H. Unger, John Wiley & Sons
2. Switching and Finite Automota Theory. Kohavi, Tata McGraw Hill

Course Outcomes:

At the end of the course the student will be able to:

CO1- Gain a knowledge of asynchronous techniques. (Cognitive- understanding)

CO2-Evalvate delays and hazards in asynchronous design. (Affective- Evaluate)

CO3 –Analyze different method for improving digital design. (Skills- analyze)

CO4- Design and optimization of NCL logic. (Skills- Create)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT640	Course Name: Electronic manufacturing Technology
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components:

   (i) Weekly Submissions (Internal assessment)   20%
   (ii) Mid-term examinations   30%
   (iii) End Semester Examination   50%

Syllabus: Overview of different technologies & future trends- (i) PCB, multilayer PCB, (ii) thin film, (iii) Thick film, (iv) Surface mount devices (v) monolithic- VLSI & MMIC (vi) packaging of semiconductor devices (vii) multichip modules & optoelectronic sub-system packaging (viii) system-on-package(ix) Micro-electro-mechanical systems & NEMS (x) Nanotechnology (xi) standards & procedures- MIL-M- 38 510F, MIL-STD-883B, ISO-9000 etc. [36 hours]

Text Books:

1. Manufacturing Technology in the Electronics Industry: An introduction, Edwards P.,Springer Netherlands, 1991
2. Handbook of Electronics Manufacturing Engineering, Bernard S. Matisoff, Springer Netherlands, 1991

Course Outcomes:

At the end of the course the student will be able to:

CO1- Gain a knowledge of different PCB layers. (Cognitive- understanding)

CO2- Understand challenges in PCB design technologies. (Cognitive - understanding)

CO3 –Analyze different method for improving packaging of chips. (Skills- analyze)

CO4- Design and optimization of system on package as per industry standards. (Skills- Create)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT642	Course Name: FPGAs Physical Design
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: Digital System Design and FPGA	
Course Type: Elective	
COURSE DURATION: 12/13/14 weeks excluding examinations	

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

    (i) Weekly Submissions (Internal assessment)   20%
    (ii) Mid-term examinations   30%
    (iii) End Semester Examination   50%

Syllabus:

Module 1: Introduction to FPGA Architectures, CLB, LUT, programming technology, routing. State of art architectures[5 hours]

Module 2: FPGA design flow, Physical design automation, Fabrication of devices, Design rules, Fabrication process and its impact on physical design, Basic data structure methods [8 Hours]

Module 3 Partitioning : Classification, Group Migration Algorithms, Simulated Annealing and Evolution, Other Partitioning algorithms, Performance driven partitioning [9 Hours]

Module 4: Floor Planning, Placement and routing algorithms: Types of Floor planning, Chip planning, pin assignment, Classification of Placement algorithms, Simulation based placement, Partitioning based placement, other placement, Global routing, Detailed routing, Clock and power routing etc. [10 Hours]

Module 5: Technology mapping for FPGAs, case studies. [5 hours]

Text Books:

1. Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, Kluwer, 1999
2. Brown, S. D., Francis, R. J., Rose, J. and Vranesic, Z G. Field programmable Gate arrays. Kluwer, 1992.
3. Betz, V., Rose, J. and Marquardt, A. Architecture and CAD for Deep-submicron FPGAs. Kluwer, 1999.
4. Trimberger, S. M. FPGA Technology. Kluwer, 1992.
5. Oldfield, J. V. and Dorf, R. C. FPGAs: Reconfigurable logic for rapid prototyping and implementation of digital systems. John Wiley, 1995

Course Outcomes:

At the end of the course the student will be able to:

CO1- Gain a knowledge of different FPGA Architectures (Cognitive- understanding)

CO2- Understand challenges in placement and routing algorithms. (Cognitive - understanding)

CO3 –Analyze different method for improving physical design. (Skills- analyze)

CO4- Evaluate Technology mapping for FPGAs (Skills- Evaluate)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT644	Course Name: Mixed Signal IC Design
Credit: 3	L-T-P: 3-0-0
Course Type: Elective	
Pre-requisite Course: Analog CMOS IC	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	50%

Syllabus:

Sample and Hold Circuits: Basic S/H circuit, effect of charge injection, compensating for charge injection, bias dependency, bias independent S/H.   [5- 8 hrs]

D/A Converter: – General considerations, Static non-idealities and Dynamic non-idealities; Current-steering DAC – Binary weighted DAC, Thermometer DAC, Design issues, Effect of Mismatches.   [9hrs]

A/D converter: – General considerations, static and dynamic non-idealities. Flash ADC – Basic architecture, Design issues, Comparator and Latch, Effect of non-idealities, Interpolative and Folding architectures. Successive Approximation ADC; Pipeline ADC. Over sampling ADC – Noise shaping, Sigma-Delta modulator. [9 hrs]

PLLs: Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, The PLL in Lock, Liberalized Small-Signal Analysis, Second-Order PLL Model , Limitations of the Second-Order Small-Signal Model, PLL Design Example [10hrs]

Text Books:

1. Behzad Razavi, "Principles of data conversion system design", S. Chand and company Ltd, 2000
2. Design of Analog CMOS Integrated Circuits: Behzad RazaviMc Graw Hill Education(India) Edition 2018
3. VLSI Design techniques for Analog and digital Circuits: *R.L. Geiger, P.E. Allen*, D. R. Holberg, OUP, (2/E) *McGraw Hill (2002)*
4. Jacob Baker, "CMOS Mixed-Signal circuit design", A John Willy & Sons, inc., publications, 2003,
5. Analysis And Design Of Analog ICs : Paul R. Gray, Paul J. Hurst Stephen H. Lewis, Robert G. Meyer, J, Willy and Sons, (4/E) (2001)

Course Outcomes:

At the end of the course the student will be able to:

CO1: Understanding working of Sample and Hold Circuits, compensation methods and bias independent design techniques.

CO2: Understanding basics of ADC, various design issues and their mitigation methods.

CO3: Understanding basics of DAC, various design issues and their mitigation methods

CO4: Understanding the PLL principle of operation, working of its component and the effects of the loop components on the system performance

CO5: Design a phase-locked loop for application as a frequency synthesizer, frequency tracking filter, and demodulator for AM, FM.

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT648	Course Name: Languages for Hardware Description, Scripting and Simulation
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

    (i) Weekly Submissions (Internal assessment)   20%

    (ii) Mid-term examinations   30%

    (iii) End Semester Examination   50%

Syllabus:

UNIT-I UNIX and SCRIPTING

Introduction to UNIX commands, Handling directories, Filters and Piping, Wildcards and Regular expression, Power Filters and Files Redirection, Working on Vi/Vim/gvim editor, Basic Shell Programming, TCL, Perl and Python Scripting language. [6 hrs]

UNIT-IIHDL Simulation and Synthesis

Synthesis and simulation using HDLs- Logic synthesis using Verilog. FSM synthesis, Continuation, Data path Synthesis, Performance driven synthesis, Types of simulation, Problem solving, Static timing analysis. Formal verification, Switch level and transistor level simulation, Problem solving, Tutorial. [8 hrs]

UNIT-IIIVLSI Design Verification (Selected Topics)

System Verilog- Introduction- Design hierarchy, Data types, Operators and language constructs, Functional coverage, Assertions, Interfaces and test bench structures, Assertions, Interfaces and test bench structures, OVM, UVM. Discussions. [8 hrs]

UNIT-IVVerilog –A and Verilog- AMS

Analog/Mixed Signal Modeling and Verification-Introduction, Analog/Mixed signal modelling using Verilog-A, Analog/Mixed signal modelling using Verilog-AMS, Event Driven Modelling: Real number modelling of Analog/Mixed blocks modelling, Analog/Digital Boundary Issues: boundary issues coverage [8 hrs]

UNIT V Advances in Scripting and System design

New softwares/languages recently used in industry. Case studies. [6hrs]

Text Books:

1. S. Sutherland, S. Davidmann, P. Flake, "System Verilog for Design (2/e)" Springer,2006.
2. M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2008.
3. H. Gerez, 'Algorithms for VLSI Design Automation', John Wiley 1999.
4. Recent literature in Electronic Design Automation Tools.
5. Z. Dr Mark, "Digital System Design with SystemVerilog", Pearson 2010;

Course Outcomes: At the end of the course the student will be able to:

CO1: execute the special features of VLSI back end and front end CAD tools and UNIX shell script

CO2: design synthesizable Verilog and VHDL code.

CO3: Application of Verilog and system Verilog in digital system

CO4: Model Analog and Mixed signal blocks using Verilog A and Verilog AMS

CO5: Understand the new scripting languages,system design softwares and EDA tools.

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT649	Course Name: Nanotechnology & Emerging Applications
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

    (i) Weekly Submissions (Internal assessment)   20%
    (ii) Mid-term examinations   30%
    (iii) End Semester Examination   50%

Syllabus:

Introduction: concept of nanotechnology, Origin of nanotechnology: change in optical, mechanical, electronic and magnetic behavior at nanoscale, Advantages of nanostructures in comparison to macrostructures, Scope of nanotechnology. **(4h)**

Categories of nanostructures and nanomaterials and their properties: Classification based on dimensionality: zero, one, two and three dimensional nanostructures:-Quantum Dots and Wells, nanowires, nanorods, nanoparticles, thin films, Carbon-based nano materials (buckyballs, nanotubes, graphene), Metallic nano materials (nanogold, nanosilver and metal oxides). Nanocomposites. Nanopolymers, Biological nanomaterials. **(8h)**

Synthesis of nanostructures and nanomaterials: Synthesis of nanoparticles, nanorods and nanowires, thin films: Ball Milling, Electrodeposition, Spray Pyrolysis, Flame Pyrolysis, Sol-Gel Processing, Solution Precipitation, Molecular Beam Epitaxy (MBE), Metal Nanocrystals by Reduction, Solvothermal Synthesis, Fundamental aspects of VLS and SLS growth, VLS growth of Nanowires, Control of the size of the nanowires, Template based synthesis, Chemical Vapor Deposition (CVD), Metal Oxide - Chemical Vapor Deposition (MOCVD), Physical vapor Deposition (PVD), Chemical vapour Deposition (CVD), DC/RF Magnetron Sputtering, Atomic layer Deposition (ALD). **(9h)**

Characterization of nanostructures and nanomaterials: Scanning Electron Microscopy (SEM), Field Emission Scanning Electron Microscopy (FESEM), High Resolution Transmission Electron Microscope (HRTEM), Scanning Tunneling Microscope (STM), Atomic Force Microscopy (AFM), X-ray Photoelectron Spectroscopy (XPS), Raman Spectroscopy, Infrared Spectroscopy, X-Ray Diffraction, Photoluminescence Spectroscopy, X-ray Fluorescence Method, Energy Dispersive Analysis of X-rays (EDAX), Thermogravimetry, Differential Thermal Analysis and Differential scanning calorimetry. **(9h)**

Applications: Application of nanotechnology in various domains: nano and molecular electronics, nano-devices like FinFETs, Tunnel-FETs, nanochemistry, nanobiotechnology, nanomedicine, nanomagnetism, nanorobotics, nanophotonics, smart nanosensors, MEMS/NEMS, nanotechnololgy for energy systems. **(6h)**

Text Books:

1. Nabok A., 'Organic and Inorganic Nanostructures', Artech House. 2005.
2. Dupas C., Houdy P., Lahmani M., "Nanoscience: Nanotechnologies and Nanophysics", Springer-Verlag Berlin Heidelberg, 2007.
3. Edelstein A S and Cammarata R C, "Nanomaterials: synthesis, Properties and Applictions", Taylor and Francis. 2012.
4. Michael Wilson, KamaliKannangara and Geoff Smith, "NANOTECHNOLOGY - Basic Science and Emerging Technologies", A CRC Press Company. D.C. 2002.;

Course Outcomes:

At the end of the course the student will be able to:

CO1: Knowledge of vast scope and capabilities of nanotechnology (Cognitive- understanding)

CO2: Acquaintance with various kinds of nanostructures and nanomaterials (Cognitive- Analyze)

CO3: Awareness of several kinds of synthesis and characterization techniques for nanostructures and nanomaterials (Cognitive- understanding)

CO4: Knowledge of applications of nanotechnology in various diverse domains.(Skills- Applying)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT652	Course Name: RF MEMS
Credit: 3	L-T-P: 3-0-0
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

    (i) Weekly Submissions (Internal assessment)   20%

    (ii) Mid-term examinations   30%

    (iii) End Semester Examination   50%

Syllabus:

RF MEMS relays and switches: Switch parameters, Actuation mechanisms, Bistable relays and micro actuators, Dynamics of switching operation. [6h]

MEMS inductors and capacitors: Micromachined inductor, Effect of inductor layout, Modeling and design issues of planar inductor, Gap tuning and area tuning capacitors, Dielectric tunable capacitors.[8h]

Micromachined RF filters: Modeling of mechanical filters, Electrostatic comb drive, Micromechanical filters using comb drives, Electrostatic coupled beam structures. [8h]

MEMS phase shifters: Types, Limitations, Switched delay lines, Micromachined transmission lines, Coplanar lines, Micromachined directional coupler and mixer.[8h]

Micromachined antennas: Microstrip antennas – design parameters, Micromachining to improve performance, Reconfigurable antennas. [6]

Text Books:

1. H.J.D.Santos, "RF MEMS Circuit Design for Wireless Communications", Artech House ,2002.
2. G.M.Rebeiz , "RF MEMS Theory , Design and Technology", wiley , 2003.
3. Stephen D Senturia, "Microsystem Design", Kluwer Academic Publishers, 2001.
4. Marc Madou, "Fundamentals of Microfabrication", CRC Press, 1997.
5. V.K.Varadan, K.J Vinoy& K.A. Jose, "RF MEMS and their Applications", Wiley,2003.
6. Gregory Kovacs, "Micromechanised Transducers Source Book", WCB McGraw Hill, Boston, 1998.
7. M H Bao, "Micromechanical Transducers, Pressure Sensors, Accelerometers and Gyroscopes" Elsevier, Newyork, 2000.

Course Outcomes:

At the end of the course the student will be able to:

CO1: Understand various parameters of RF MEMS Switch and its actuation

CO2: Model and design inductor and capacitors

CO3: Design Micromechanical filters

CO4: Understand the various aspects of design of MEMS phase shifters and its application

CO5: Analyze the performance of microstrip antennas

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT654	Course Name: RF Integrated Circuits
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: Analog and digital CMOS IC	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%	
(ii) Mid-term examinations	30%	
(iii) End Semester Examination	50%	

Syllabus:

Fundamental concepts in RF Design – harmonics, gain compression, desensitization, blocking, cross modulation, intermodulation, inter symbol interference, noise figure, Friis formula, sensitivity and dynamic range; Receiver architectures – heterodyne receivers, homodyne receivers, image-reject receivers, digital-IF receivers and subsampling receivers; Transmitter architectures – direct-conversion transmitters, two-step transmitters; Low noise amplifier (LNA) – general considerations, input matching, CMOS LNAs; Down conversion mixers – general considerations, spur-chart, CMOS mixers; Oscillators – Basic topologies, VCO, phase noise, CMOS LC oscillators; PLLs – Basic concepts, phase noise in PLLs, different architectures.   [36 h]

Text Books:

1. Behzad Razavi, RF Microelectronics, Prentice Hall PTR, 1997
2. Thomas H. Lee, The design of CMOS radio-frequency integrated circuit, Cambridge University Press, 2006
3. Chris Bowick, RF Circuit Design, Newnes, 2007.

Course Outcomes:

At the end of the course the student will be able to:

CO1: Knowledge of basic concepts in RF integrated circuit design (Cognitive- understanding)

CO2: Acquaintance with various architectures of receivers and transmitters (Cognitive- Analyze)

CO3: Awareness of several concepts of low noise amplifiers (Cognitive- understanding)

CO4: Knowledge of applications of mixers, oscillators and PLLs. (Skills- Applying)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT656	Course Name: Adaptive Signal Processing
Credit: 3	L-T-P: 3-0-0
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

    (i) Weekly Submissions (Internal assessment)   20%
    (ii) Mid-term examinations   30%
    (iii) End Semester Examination   50%

Syllabus:

Adaptive Filter Structures and Algorithms:

Introduction to Adaptive systems, Adaptive Linear combiner, Minimum Mean-Square Error, Wiener-Hopf Equation, Error Performance Surface, LMS algorithm, Convergence of weight vector, Learning Curve, FX-LMS algorithm (Filtered X-LMS) and its application to ANC, Types of LMS, RLS algorithm, Matrix Inverse Lemma for RLS, Computational complexity of LMS and RLS, Convergence Analysis.

IIR-LMS, Lattice Filter, FIR to Lattice conversion and vice-versa, Adaptive Lattice Filter

Kalman Filter, Adaptive Kalman Filter

Transformed domain adaptive filtering : Block Linear, Block Circular

Filter Banks and multi-rate signal processing

Distributed signal Processing : Incremental LMS, Diffusion LMS

Applications:

Direct Modelling or System Identification, Inverse Adaptive Modelling (Equalization), Adaptive Noise Cancellation, Adaptive filters for time series and stock market prediction, Biomedical Applications (Cancellation of 50-Hz interference in Electro-Cardiography, Cancelling donor heart interference in heart-transplant electrocardiography, Cancelling Maternal ECG in Fetal Electrocardiography), Echo Cancellation in Long distance Telephone Circuits, Adaptive self tuning filter, Adaptive line enhancer, Adaptive filters for classification and data mining. [36h]

Text Books:

1. B. Widrow and S. D. Stearns : Adaptive Signal Processing, Prentice Hall.
2. D. G. Manolakis, V. K. Ingle, S. M. Kogon : Statistical and Adaptive Signal Processing, McGraw Hill.
3. S. S. Haykin : Adaptive Filter Theory, 4th Edition, Prentice Hall.
4. A. H. Sayed : Fundamentals of Adaptive Filtering, John Wiley & Sons.

Course Outcomes:

At the end of the course the student will be able to:

CO1 : To learn the characteristics of adaptive system architecture and analyze Wiener-Hopf Equation.

CO2 : To understand the machine learning algorithms including LMS, RLS, Fx-LMS etc.

CO3 : To learn the adaptive structures like : Adaptive Lattice Filter, Kalman Filter, Transformed domain adaptive filtering, Filter Banks.

CO4 : To explore the applications of adaptive signal techniques to System Identification, Channel Equalization, time series prediction etc.

CO5 : To develop MATLAB programming skills for adaptive systems.

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT658	Course Name: Current-Mode Analog Signal Processing
Credit: 3	L-T-P: 3-0-0
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

    (i) Weekly Submissions (Internal assessment)   20%

    (ii) Mid-term examinations   30%

    (iii) End Semester Examination   50%

Syllabus:

Current-mode (CM) Processing, Advantages over voltage-mode processing; Supply-current Sensing, Translinear circuits, Current- feedback opamps, Current Conveyors, Current-mode filters, Log domain filters, Current-mode Instrumentation Amplifiers and Precision Rectifiers, Current-mode Sinusoidal Oscillators and Function Generators, Issues in Current-Output Sensing, Advanced Current-mode building blocks: Current-Controlled Conveyor (CCCII), Current-Differencing Transconductance Amplifier (CDTA), etc. and their applications to high frequency, analog signal processing applications. [36h]

Text Books:

1. Esteban Tlelo-Cuautle, "*Integrated Circuits for Analog Signal Processing*," Springer,2012, ISBN: 1461413834, 9781461413837.
2. Chris Toumazou, F. J. Lidgey, David Haigh, "*Analogue IC Design: The Current-mode Approach*," in Circuits, Devices and Systems, Issue 2 of IEE circuits and systems series, IET, 1993, ISBN: 0863412971, 9780863412974.
3. Fei Yuan, "*CMOS Current-Mode Circuits for Data Communications*," in Analog Circuits and Signal Processing, Springer, 2010, ISBN: 1441939997, 9781441939999.
4. P. V. Ananda Mohan, "*Current-Mode VLSI Analog Filters: Design and Applications*," Springer, 2003, ISBN: 0817642773, 9780817642778.
5. Latest research papers on the topics mentioned in the syllabus

Course Outcomes:

At the end of the course the student will be able to:

CO1- Gain a knowledge of different current mode sensing. (Cognitive- understanding)

CO2- Understand challenges in current-mode signal processing technologies. (Cognitive - understanding)

CO3 –Analyze different method for improving current-mode analog circuits. (Skills- analyze)

CO4- Design and optimization of Current-Differencing Transconductance Amplifier. (Skills- Create)

Program: M. Tech. (VLSI Design)	Department: Electronics & Communication Engineering
Course Code: ECT703	Course Name: CAD Algorithms for Synthesis of VLSI Systems
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: none	
Course Type: Elective	

Syllabus: Unit 1: **Introduction to CAD Algorithms**

Role of CAD in digital system design, levels of design, modeling & description and support of languages, RTL, gate and system level synthesis; Technological alternatives and technology mapping   [6hrs]

Unit 2: **CAD Tools for synthesis**

CAD tools for synthesis, optimization, simulation and verification of design at various levels as well as for special realizations and structures such as microprogrammes, PLAs, gate arrays etc. Technology mapping for FPGAs. Low power issues in high level synthesis and logic synthesis. [8 hrs]

Unit 3: **Architectural-Level Synthesis and Optimization**

Architectural Synthesis, Scheduling, Data path synthesis and control unit synthesis, scheduling algorithm, Resource Sharing and Binding [8 hrs]

Unit 4: **Logic-Level Synthesis and Optimization**

Two-Level Combinational Logic Optimization, Multiple-Level Combinational Logic Optimization, Sequential Logic Optimization [8 hrs]

Unit 5: **CAD Algorithms for VLSI Physical Design**

Introduction to VLSI Physical Design flow. Circuit partitioning, placement and routing algorithms. Design Rule-verification. Circuit Compaction; Circuit Extraction and post layout simulation. FPGA design flow- partitioning, placement and routing algorithms. Deep sub-micron issues; interconnects modeling and synthesis

[6 hrs]

Text Books:

1. G. D. Micheli. Synthesis and optimization of digital systems.
2. Dutt, N. D. and Gajski, D. D. High level synthesis, Kluwer, 2000.
3. T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms," McGraw-Hill, 1990.
4. N. Deo. Graph Theory, PH India.
5. Sait, S. M. and Youssef, H. VLSI Physical design automation. IEEE press, 1995.
6. Sherwani, N. VLSI physical design automation. Kluwer, 1999.

Course Outcomes:

CO1: Is able to grasp various operations on graphs, clique, coloring, partitioning etc& apply graph algorithms and its applications into Boolean function representation (Skills- Apply)

CO2: Is able to grasp graph models for architecture representation (Cognitive- understanding)

CO3: Is able to analyze & implement two level/Multilevel/ sequential logic synthesis algorithms

(approximate & exact algorithms) (skills- Analyze)

CO4: Is able to analyze & implement library binding algorithms- FSM equivalence & optimization (skills- Evaluate)

CO5: To able to grasp core concept of VLSI Physical Design algorithms. (Cognitive- Apply)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT643	Course Name: Special Modules in VLSI - I
Credit: 1	L-T-P: 1-0-0

COURSE DURATION: 12/13/14 weeks excluding examinations

Course Type: Elective

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	40%
(ii) Mid-term examinations	20%
(iii) End Semester Examination	40%

Syllabus:

Current advances in VLSI Design as defined by instructor- Following is suggested but not restrictive:

Novel devices and relevant materials; Device & Technology CAD; Sensors & bio-Sensors [12-14h]

References:

Current literature from quality journals & magazines such as IEEE, ACM, IET etc. & others;

Books on niche areas;

Course Outcomes:

At the end of the course the student will be able to:

CO1: To analyze & implement device design/structure (simulation/fabrication) (Skills, Evaluate)

CO2: To enable her/him to perform research problem solution in a niche & socially relevant area (Affective, creative)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT645	Course Name: Special Modules in VLSI - II
Credit: 1	L-T-P: 1-0-0

COURSE DURATION: 12/13/14 weeks excluding examinations

Course Type: Elective

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	40%
(ii) Mid-term examinations	20%
(iii) End Semester Examination	40%

Syllabus:

Current advances in VLSI Design as defined by instructor- Following is suggested but not restrictive:
Circuits- low energy, high performance digital circuits; energy harvesting, sensor conditioning, data conversion, very high speed mixed signal [12-14h]

References:

Current literature from quality journals & magazines such as IEEE, ACM, IET etc. & others;

Books on niche areas;

Course Outcomes:

At the end of the course the student will be able to:

CO1: To analyze & implement high performance analog and digital circuits (simulation/fabrication) (Skills, Evaluate)

CO2: To enable her/him to perform research problem solution in a niche & socially relevant area (Affective, creative)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT646	Course Name: Special Modules in VLSI - III
Credit: 1	L-T-P: 1-0-0
COURSE DURATION: 12/13/14 weeks excluding examinations	
Course Type: Elective	

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade). will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	40%	
(ii) Mid-term examinations	20%	
(iii) End Semester Examination	40%	

Syllabus:

Current advances in VLSI Design as defined by instructor- Following is suggested but not restrictive:
Systems- SoC, neuromorphic computing, Ubiquitous computing/wearable computing [12-14h]

References:

Current literature from quality journals & magazines such as IEEE, ACM, IET etc. & others;

Books on niche areas;

Course Outcomes:

At the end of the course the student will be able to:

CO1: To analyze & implement computing methodologies with system perspective (simulation/fabrication) (Skills, Evaluate)

CO2: To enable her/him to perform research problem solution in a niche & socially relevant area (Affective, creative)

Program: M. Tech.	Department: Electronics & Communication Engineering
Course Code: ECT647	Course Name: Special Modules in VLSI - IV
Credit: 1	L-T-P: 1-0-0
COURSE DURATION: 12/13/14 weeks excluding examinations	
Course Type: Elective	

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	40%
(ii) Mid-term examinations	20%
(iii) End Semester Examination	40%

Syllabus:

Current advances in VLSI Design as defined by instructor- Following is suggested but not restrictive: Electronic design Automation- algorithms, methodologies, tools- industrial & open source [12-14h]

Text Books:

Current literature from quality journals & magazines such as IEEE, ACM, IET etc. & others;

Books on niche areas;

Course Outcomes:

At the end of the course the student will be able to:

CO1: To gain hands-on knowledge of EDA tools, techniques and methodologies (simulation/fabrication) (Skills, Evaluate)

CO2: To enable her/him to perform research problem solution in a niche & socially relevant area (Affective, creative)

Program: M. Tech. (VLSI Design)	Department: Electronics & Communication Engineering
Course Code: ECT992	Course Name: Mathematical Methods and techniques for Electronics & Communication Technologists-II
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	20%	
(ii) Mid-term examinations	30%	
(iii) End Semester Examination	50%	

Syllabus:

[The following contents intend to cover implicit application to and exemplification through ECE problems in Electronic systems/Cognitive-systems domain such as reduced order polynomials, order reduction of a transfer function, sparse matrix based solution of large systems, discrete structures, implementation of search algorithms for design space exploration, and computer arithmetic implementation along with probabilistic reasoning for AI]

A.   (i) (a) Large Matrix analysis and large Eigen value problem– Groups, fields and rings; vector spaces; basis & dimensions; canonical forms; inner product spaces- orthogonalization, Gram-Schmidt orthogonalization, unitary operators, change of orthonormal basis, diagonalization; (b) Eigenvalues & eigen vectors- Gerschghorin theorem, iterative method, Sturm sequence, QR method, introduction to large Eigen value problems.   08 Hrs.

(ii) Reduced order modelling of systems- Taylor's polynomial, least square approximation. Chebyshev series/polynomial, splines, Pade& rational approximation   04 Hrs.

B.   Discrete Structures, graphs, algorithms & Combinatorial optimization- counting methods, algorithm analysis, graph algorithms, dynamic algorithms, randomized algorithms, probabilistic algorithms. combinatorial optimization16 Hrs.

C.   (i) Number theory & computer arithmetic- unconventional number systems, residue number system, logarithmic number system, Chinese remainder theorem; fast evaluation of elementary& transcendental arithmetic functions.   06 Hrs.

(ii) Preface to AI- first order logic & inferencing, uncertainty, probabilistic reasoning systems, making decisions under uncertainty;   **08 Hrs.**

Text Books:

1. Schaum's outline on Linear Algebra. McGraw Hill
2. Topics in Algebra, I. N. Herstein, Wiley.
3. Gerald, C F; Wheatley P O; Applied Numerical Analysis, Pearson, 2017
4. Theory and Applications of Numerical Analysis, G. M. Phillips, Peter J. Taylor, Academic press
5. Advanced Model Order Reduction Techniques in VLSI Design, Sheldon Tan. Lei He, Cambridge Univ. Press, 2007.
6. Cormen, Rivest, Leiserson, Introduction to Algorithms, PHI
7. Combinatorial optimization. Papadimitriou and Steiglitz, PHI (I)
8. Russel and Norvig- Artificial Intelligence: A Modern Approach, Pearson, 3rd Ed. 2017
9. Israel Koren, Computer Arithmetic- Academic Press
10. Model Order Reduction: Theory, Research Aspects and Applications edited by W. H. A. Schilders, Henk A. Van Der Vorst, Joost Rommes, Springer.

11. Discrete Structures, Schaum outline

Further Text Books

1. MODEL ORDER REDUCTION TECHNIQUES WITH APPLICATIONS IN ELECTRICAL ENGINEERING, Luigi FORTUNA, Guiseppe NUNNARI, Antonio GALLO, Springer, 1992.
2. Y. Saad, Numerical methods for large Eigenvalue problems. www.umn.edu
3. Matrix Analysis & linear algebra, Meyer, SIAM
4. H. A. van der Vorst, Iterative methods for large linear systems, citeseerx.ist.psu.edu

Course Outcomes:

CO1.   Is able to grasp core concepts, basic tenets of linear algebraic structures- groups, fields and rings;vector spaces (knowledge)

CO2.   Is able to grasp features, properties and operations on vector spaces- orthogonalization, change of basis, diagonalization (knowledge)

CO3.   Is able to learn & apply problem solving for computing eigen values and eigen vectoraetc. (Thinking, skills)

CO4.   Is able to demonstrate application of algorithms (Gerschgorin, Sturm sequence method, QR method) for eigen value computation/estimation and MATLAB validation(skills)

CO5.   Is able to describe algorithms for function approximation (rational, Chebychev, Pade etc.) using MATLAB (skills)

CO6.   Develops appreciation for combinatorial optimization algorithms, AI probabilistic approaches & implements through MATLAB/C++ (skills)

Program: M.Tech	Department: *Electronics & Comm. Engg.*
Course Code ECT657	Course Name: VLSI Signal Processing Architectures
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

- (i) Weekly Submissions (Internal assessment) 20%
- (ii) Mid-term examinations 30%
- (iii) End Semester Examination 50%

Unit 1: **Introduction to VLSI DSP Sytems**

Need of VLSI DSP algorithms. main DSP Blocks and typical DSP Algorithms. Fixed point /Floating point Representation; Floating point Arithmetic Implementation, Architectures of Adders/Multipliers; CORDIC, representation of DSP algorithms: Block Diagram, signal flow graph, data flow graph, dependence graph.   [8 hrs]

Unit 2: **Iteration Bound**

Data flow graph representations, loop bound and iteration bound, longest path matrix algorithm, iteration bound of Multirate data flow graphs   [6 hrs]

Unit 3: **Pipelining and Parallel Processing:**

Pipelining and parallel processing of FIR digital filters, pipeline interleaving in digital filters: signal and multichannel interleaving [4 hrs]

Unit 4: **Retiming, Unfolding and Folding:**

retiming techniques; algorithm for unfolding. Folding transformation. Techniques of retiming, Unfolding & Folding   [10 hrs]

Unit 5: **Systolic Array Architecture**

Systolic Array Architecture: Methodology of systolic array architecture, FIR based Systolic Array, Selection of Scheduling Vector, Matrix multiplication of systolic array [6 hrs]

Unit 6: **Low power Design**

Theoretical background , Scaling v/s power consumption, power analysis, Power reduction techniques, Power estimation approach [4 hrs]

Reading Text Books

- VLSI Digital Signal Processing System : : Design and implementation by K.K. Parhi
- Digital Signal Processing with Field Programmable Gate Arrays Uwe Meyer-Baese , Springer.
- FPGA-based Implementation of Signal Processing Systems. by Roger Woods, John Mcallister, WILEY

CO1	To understand Graphical representation of DSP algorithms and Mapping algorithms into Architectures (Cognitive/Skills- Apply)
CO2	To study architecture for real time systems and parallel and pipelining for Low power design (Cognitive-Remembering)
CO3	To be aware of systolic Array architecture and methodology for developing Architectures (Cognitive-Understanding)
CO4	To know different signal processing modules as convolution technique, retiming concept. folding /unfolding Transformation and CORDIC architecture. (Cognitive- Analyse)
CO5	To implement different low power Design techniques. (Skills- evaluate)

Program: M Tech (Embedded System)	Department: Electronics & Communication Engineering
Course Code: ECT 736	Course Name: Medical Engineering & Systems
Credit:3	L-T-P:3-0-0
Course Type: Elective	

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

- (i) Weekly Submissions (Internal assessment) — 20%
- (ii) Mid-term examinations — 30%
- (iii) End Semester Examination — 50%

Syllabus: Module 1: Physiological Signal Processing

Physiology: Basics of ECG Signal and its Acquisition, Electrical activity of heart, ECG Waveform, Interpretation of ECG, Introduction of EEG Signal, EEG Acquisition, Neural activity in the brain, Signal Propagation in the brain, EMG signal, EMG recording, Signal processing and Filtering of EEG, ECG, EMG etc. **[8 Hours]**

Module 2: Wearable Device and Healthcare Technologies

Health monitoring with wearable sensors, Wearable electrodes of ECG, EEG & EMG, Accelerometer, Glucose sensing device, Smart healthcare components- cHealth, eHealth and mHealth. Role of IoT in Healthcare, Electronics Health Records, Concept of Bioinformatics, Security and Privacy of Health records **[8 Hours]**

Module 3: Machine Learning for Health information

Data & Modelling of Health information, Basics concepts of ML, Role of ML for Healthcare, Feature Extraction of real-world signals as speech, audio, text, image, video., Pre-processing Requirements of signals, Noise and artifacts, information retrieval, Optimization, Regression, Classification, Unsupervised Learning for Health data, Pattern Recognition, Gaussian models, Time series modelling. **[10 Hours]**

Module 4: Deep learning for healthcare

Basics of DL, MLP, Back Prorogation, Convolutional Neural Networks & Recurrent Neural network for digital health, Forward and Backward propagations, Architectures for sequence to sequence and sequence to vector mapping, Models for Healthcare using deep, recurrent and deep networks, LSTM, Medical Image analysis, Need for Deep Learning & Neuroimaging, Object Detection, Segmentation, Deep learning models. **[8 Hours]**

Module 5: Medical Devices and Systems

Risks of Integration and Healthcare Systems Testing & Evaluation, Vitro/Vivo testing, Regulatory requirements of medical devices, Standards of medical device, quality assurance Medical Device Classification, Risk management system for medical devices, Certification of medical device, Ethical regulation of medical devices & systems, Medical Devices regulation in India, USA and other countries. **[4 Hours]**

Text Books:

1. Introduction to Biomedical Engineering by John Enderle, Joseph Bronzino Academic Press
2. **Biomedical Engineering: Bridging Medicine and Technology** by W. Mark Saltzman, Cambridge
3. **Machine Learning and Analytics in Healthcare Systems: Principles and Applications (Green Engineering and Technology)** by Himani Bansal, Balamurugan Balusamy, et al., CRC.
4. **Machine Learning in Medicine** by Ayman El-Baz and Jasjit S. Suri, Chapman & Hall/CRC Health Informatics,
5. Demystifying Big Data, Machine Learning, and Deep Learning for Healthcare Analytics by Pradeep N, Sandeep Kautish, et al., Academic Press

Course Outcomes:

CO1: To understand the basic concepts of various physiological signals and their processing (Knowledge)

CO2: To understand and design the medical devices and technologies for healthcare (Cognitive, Understanding)

CO3: To learn and develop the machine learning models for healthcare applications (Affective, creative)

CO4: To aware of various risk, ethical and regulatory rules for medical devices & systems (Cognitive- Analytic)